



FORM PTO-1449	SERIAL NO.: 10/175,139	DOCKET NO. 09799940-0120-001 Cypress: PM99002
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	FILING DATE February 7, 2002	GROUP ART UNIT 1765-2811
(use several sheets if necessary)	APPLICANT(S): Tinghao F. Wang	

REFERENCE DESIGNATION		U.S. PATENT DOCUMENTS				
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS/ SUBCLASS	FILING DATE
qs	A1	5,645,683	07-08-1997	H. Miyamoto	156/643.1	02-07-1995
qs	A2	6,087,264	07-11-2000	H-S Shin, et al.	438/706	01-13-1997

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FOREIGN PATENT DOCUMENTS						
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS/ SUBCLASS	TRANSLATION YES NO

	EXAMINER INITIAL	OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)
qs	C1	Chang, C.P., F.P. Klemens, H.L. Maynard, T.C. Lee, et al. 1997. "Polycide gate etching using a helical resonator on an applied materials precision 5000 platform", <i>J. Vac. Sci. Technol.</i> , 15(3):646-651.
	C2	Chinn, J.D., D. Buseck, Th. Lill, N. Padmapani, 1996. "Influences on film selectivities in the etching of polycide gates", <i>Electrochem. Soc. Proc.</i> , 96(12):313-321.
	C3	Grossman, E., A. Bensaoula, and A. Ignatiev, 1987. "An XPS Study of XeF ₂ Dry Etching of Tungsten Silicide", <i>Surface Science</i> , 197:99-108.
	C4	Kim, S-J, K. Shin, and H-K Park, 1995. "Dry Post-Etch Treatment Using SF ₆ Chemistry for 0.2 μm Contact Hole", <i>Jpn. J. Appl. Phys.</i> 34:5001-5005.
	C5	Langley, R.C., D.S. Becker, and G.W. Grynkeiwich, 1989. "One-Chamber Polycide Sandwich Etching", <i>Semicond. Int'l</i> , pp. 95-97.
	C6	Lee, R-L and F.L. Terry, Jr., 1991. "Reactive-ion etching of tungsten silicide using NF ₃ gas mixtures", <i>J. Vac. Sci. Technol. B.</i> , 9(6):2747-2751.
qs	C7	Maruyama, T., N. Fujiwara, M. Yoneda, K. Tsukamoto and T. Banjo, 1994. "Mechanism of Reactive Ion Etching Lag in WSi ₂ Etching Using Electron

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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.



FORM PTO-1449	SERIAL NO. 10/071,809	DOCKET NO. 09799940-0120-001 Cypress: PM99002
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	FILING DATE February 7, 2002	GROUP ART UNIT 1765 28TT
(use several sheets if necessary)	APPLICANT(S): Tinghao F. Wang	

EXAMINER INITIAL	OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)
	Cyclotron Resonance Plasma", <i>Jpn. J. Appl. Phys.</i> 33:2170-2174.
q/c	C8 Nojiri, K., K. Tsunokuni and K. Yamazaki, 1996. "High rate and highly selective anisotropic etching for WSi _x /poly-Si using electron cyclotron resonance plasma", <i>J. Vac. Sci. Technol. B</i> , 14(3)1791-1795.
	C9 Nowicki, R.S., C. Fuhs and P. Geraghty, 1990. "Comparison of Integrated <u>in situ</u> Rie Preclean Processes for CVD Tungsten Silicide Deposition Done in a Cluster Tool", <i>Semiconductor Mfg. Sci. Symp.</i> , Abstract only.
	C10 Nowicki, R.S., P. Geraghty and C. Fuhs, "Integration of an <u>in situ</u> Rie Preclean with a CVD Tungsten Silicide Deposition Process", VMIC Conference, June 1990, pp. 462-467.
	C11 Oehrlein, G.S. and J.L. Lindstöm, 1989. "Competitive reactions of fluorine and oxygen with W, WSi ₂ , and Si surfaces in reactive ion etching using CF ₄ /O ₂ ", <i>Amer. Vacuum Soc.</i> , 7(3)1035-1041.
	C12 Olson, Dr. K., L. McCulloch and Dr. J. Liu, 1996. "Production Worthy 0.25 μm Polycide Gate Etch System", IEEE/SEMI Adv. Semiconductor Mfg. Conference, pp. 321-327.
	C13 Pan, P. and L. Liu, 1997. "Formation and mechanism of dimple/pit on Si substrate during WSi _x /poly-Si gate stack etch", <i>J. Vac. Sci. Technol. B</i> , 15(5)1752-1757.
	C14 Pan, S.S. Xu and D. Podlesnik, 1997. "Decoupled Plasma Source Technology: Process Region Choices for Silicide Etching", <i>Jpn. J. Appl. Phys.</i> , 36:2514-2520.
	C15 Pan, W.S. and A.J. Steckl, 1988. "Selective reactive ion etching of tungsten films in CHF ₃ and other fluorinated gases", <i>J. Vac. Sci. Technol. B</i> , 6(4)1073-1080.
	C16 Parks, J.M. and R.J. Jaccodine, 1991. "Plasma Etching of Tungsten Polycide Structures Using NF ₃ -Mixed Halocarbon Etchants", <i>J. Electrochem. Soc.</i> , 138(9)2736-2741.
q/c	C17 Philipossian, A., M. Moinpour, R. Wilkinson and V.H.C. Watt, 1995. "Investigation of Pre-Tungsten Silicide Deposition Wet Chemical Processing", <i>Mat. Res. Soc. Symp. Proc.</i> , 386:75-82.
	C18 Sakiyama, K., Y. Matsubara and R. Ihoue, 1985. Statement of relevancy for

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EXAMINER INITIAL	OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)
go	"Tungsten Silicide Gate MOS LSI Process" and copy of article in Japanese, <i>Sharp Tech. Report</i> , 31:55-61.
C19	Shiozaki, K., K. Mitsuhashi, K. Ohtake and M. Koba, 1987. "Low Resistive, High Aspect Ratio Via-Hole Filling System Completely Planarized by Selective W Deposition and Subsequent Etch-Back", <i>Abstracts of 19th Conference on Solid State Devices and Materials</i> , Tokyo, pp. 435-438.
C20	Shul, R.J., M.E. Sherwin, A.G. Baca and D.J. Rieger, 1996. "Etching of sub-0.5 μ m W/WSi _x bilayer gates", <i>Electronic Letters</i> , 32(1):70-71.
C21	Tachi, S., K. Tsujimoto, S. Arai, H. Kawakami and S. Okudaira, 1988. "Low Temperature Microwave Plasma Etching", <i>Abstracts of the 20th Conf. On Solid State Devices and Materials</i> , pp. 553-556.
go	C22 Wilson, Dr. R., C. Quinn, B. McDonnell, Dr. S. Blackstone, and Dr. K. Yallup, 1995. "Bonded and Trenched SOI with Buried Silicide Layers", <i>Electrochem. Soc. Proc.</i> , 95(7):535-545.

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